	Application No.	Applicant(s)	
Notice of Allowability	09/751,163	STORINO ET AL.	
	Examiner	Art Unit	-
	Khiem D Nguyen	2823	
The MAILING DATE f this communication appe All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI- of the Office or upon petition by the applicant. See 37 CFR 1.313 1. This communication is responsive to 06/11/04.	ars on the cover sheet wa (OR REMAINS) CLOSED in or other appropriate common GHTS. This application is	ith the correspondence address n this application. If not included unication will be mailed in due course.	THIS initiativ
The allowed claim(s) is/are $\frac{7-16}{1}$.			
3. A The drawings filed on 29 December 2000 are accepted by	the Examiner.		
 Acknowledgment is made of a claim for foreign priority und a) ☐ All b) ☐ Some* c) ☐ None of the: 	er 35 U.S.C. § 119(a)-(d) c	r (f).	
1. Certified copies of the priority documents have been received.			
2. Certified copies of the priority documents have been received in Application No			
 Copies of the certified copies of the priority doc International Bureau (PCT Rule 17.2(a)). 	uments have been receive	d in this national stage application fron	n th
* Certified copies not received:	-do- 25 U.O.O. \$ 440(-) (b-		
5. Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application). (a) The translation of the foreign language provisional application has been received.			
6. Acknowledgment is made of a claim for domestic priority ur			
Applicant has THREE MONTHS FROM THE "MAILING DATE" of below. Failure to timely comply will result in ABANDONMENT of to the submarked of the su	this application. THIS THE itted. Note the attached EX	REE-MONTH PERIOD IS NOT EXTEN AMINER'S AMENDMENT OF NOTICE	IDABLE
 8. CORRECTED DRAWINGS must be submitted. (a) including changes required by the Notice of Draftspers 1) hereto or 2) to Paper No. (b) including changes required by the proposed drawing c (c) including changes required by the attached Examiner's 	correction filed, whi	ch has been approved by the Examine	
Identifying Indicia such as the application number (see 37 CFR 1. each sheet.	84(c)) should be written on t	he drawings in the front (not the back) o	f
9. DEPOSIT OF and/or INFORMATION about the depose attached Examiner's comment regarding REQUIREMENT FOR THE	sit of BIOLOGICAL MAT HE DEPOSIT OF BIOLOGI	ERIAL must be submitted. Note the CAL MATERIAL.	ı
Attachment(s)			
 1 □ Notice of References Cited (PTO-892) 3 □ Notice of Draftperson's Patent Drawing Review (PTO-948) 5 □ Information Disclosure Statements (PTO-1449), Paper No 7 □ Examiner's Comment Regarding R quirement for Deposit of Biological Material 	4□ Interviev 6□ Examine	of Informal Patent Application (PTO-15, w Summary (PTO-413), Paper No er's Amendment/Comment er's Statement of Reasons for Allowan	

÷ 44.

Application/Control Number: 09/751,163

Art Unit: 2823

DETAILED ACTION

Allowable Subject Matter

Claims 7-16 are allowed.

Reasons For Allowance

The following is a statement of reasons for the indication of allowable subject matter: The prior art taken alone or in combination neither discloses nor makes obvious the instant process of claims as a whole. Specifically, the prior art of record, Bosshart (U.S. Patent 6,049,231) discloses a logic circuit being adapted to receive an input signal and a clock signal, the method comprising: controlling the conduction of an active discharging device with the input signal (FIG. 4, INPUTS₂₆) wherein the discharging device (FIG. 4, 26_{DT}) being coupled to an intermediate node of the logic circuit (FIG. 4, 26_L) (col. 8, line 53 to col. 10, line 17) but fails to teach or suggest the Applicant's steps of provide a plurality of stacked SOI Metal Oxide Semiconductor (MOS) transistors interconnect to define a common node and an intermediate node, wherein the plurality of stacked SOI MOS transistors is controlled by a plurality of inputs; a common node is coupled to a pre-charging device; an intermediate node is in a path between the common node and a voltage source, the path defined by the plurality of stacked SOI MOS transistors; the intermediate node is coupled to the common node by at least a first of the plurality of stacked SOI MOS transistors; and the active discharging transistor is controlled by at least one of the plurality of inputs, the active discharging transistor defining a discharged path between the intermediate node and the voltage source, the method comprising: controlling the conduction of the active discharging transistor during Art Unit: 2823

a pre-charge cycle; and actively discharging the intermediate node, whereby the parasitic bipolar transistors are deactivated and the charge at the intermediate node is maintained at a predetermined level as recited in the independent claim 7, lines 3-19.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N. June 23, 2004

W. DAVID COLEMAN PRIMARY EXAMINER